Amendments to the Specification:

Please replace the paragraph beginning at page 6, line 4 with the following amended paragraph:

> In accordance with the invention, two or more measurements are made on the same workpiece, during fabrication of the workpiece, and one of the measurements is used to calibrate another of the measurements. In one embodiment, each measurement is made employing a different process, and the measurements are used together to determine a property (also called "property of interest") of the workpiece. The multiple measurements may be made at two or more locations on the workpiece that are separated from one another, or alternatively even at the same location as long as different measurement processes are used. If the same process is used, the measurements are made at different locations.

Please replace the paragraph beginning at page 9, line 24 with the following amended paragraph:

> System 100 also includes a metrology tool 103 that measures various material properties in a patterned wafer 106. Although wafer 106 is illustrated as having been polished, metrology tool 103 may be used even with unpolished wafers 105, as illustrated by path 109 in FIG. 1B[[)]].

Please replace the paragraph beginning at page 17, line 17 with the following amended paragraph:

> As noted above, in one embodiment, a property of a semiconductor substrate is measured by system 100 (FIG. 1B) as described herein. Specifically, system 100 uses a first measurement device 103A to measure (see act 110 in FIG. 2A) a number of properties of the

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semiconductor substrate. Next, system 100 uses (see act 111 in FIG. 2A) a simulator 103C to generate a simulated value of a to-be-measured signal, based on a predetermined value of the property of interest (e.g. a value identified in the specification), and also based on values of properties (other than the property of interest) that can affect the to-be-measured signal. The values of properties (other than the property of interest) are measured by the first measurement device 103A, for use by the simulator. In this embodiment, the simulator is repeatedly operated (see a loop formed by acts 112, 113 and [[110]] 111), so that a number of simulated values are generated for a corresponding number of predetermined values (which may be selected to cover a range of values for the property of interest permitted by the specification).

Please replace the paragraph beginning at page 18, line 23 with the following amended paragraph:

Thereafter, computer 103C checks if the property value matches the specifications (see act 160 in FIG. 2A), and if so, the semiconductor substrate is processed further. If the property value does not match the specifications, computer 103C drives a control signal to, for example, layer formation apparatus 101F on line 107 and/or to chemical mechanical polisher 102 on line 108, for process control. Note that even when a property value matches the specifications, if the property value falls within a predetermined range, process control may be performed (although the semiconductor substrate is not discarded) e.g. to correct an upcoming problem.

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Please replace the paragraph beginning at page 19, line 10 with the following amended paragraph:

An alternative embodiment includes use of a look-up table based on externally generated values by another computer (when computation time is long) or based on empirical values or fits to empirical values. In another embodiment illustrated in FIG. 2B, the above-described simulation is not automatically repeated (in the loop formed by acts 112, 113 and [[110]] 111), and instead, a measured signal from the second process (see act 171 in FIG. 2B) is compared (see act 173 in FIG. 2B) with a simulated value [[()] generated by the simulator[[)]] (see act 172 in FIG. 2B), which is based on a predetermined value for the property as defined by the specification. If there is no match, the simulator is operated again, with another predetermined value of the property of interest (see act [[173]] 174 in FIG. 2B), until a match is found. If there is a match, a value of the property of the region is computed (see act 175 in FIG. 2B), based on the predetermined value that produced the matching simulated value.

Please replace the paragraph beginning at page 35, line 5 with the following amended paragraph:

In one application of a measurement as described herein, a wafer requires a next level of metal interconnection. The wafer goes into process module 101 (FIG. [[18]] 1B), where an interconnect layer is formed, including dielectric stack deposition, groove etching, backfill and polishing. The wafer, with the completed additional interconnect layer, is measured in system 103 that applies the high resolution dielectric measurement to determine that the polishing process has been successfully completed. Results of measurements performed by system 103 are transferred to computer 103C. In the event that results are judged unacceptable (for

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example, because erosion is too deep), signals are sent to process module 101 to alter or halt the process to enable correction of the problem.

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